ALPIDE pixel chip development for the upgrade of the ALICE Inner Tracking System

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OUTLINE

- The ALICE experiment at CERN
- Upgrade of the Inner Tracking System (ITS)
- Pixel chip development: ALPIDE status & results
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THE ALICE EXPERIMENT

- ALICE (A Large Ion Collider Experiment) is the experiment at CERN LHC dedicated to the study of the Quark-Gluon Plasma (QGP) state of matter.

Present Inner Tracking System (ITS)

Silicon Pixel Detector (SPD)

Silicon Drift Detector (SDD)

Silicon Strip Detector (SSD)
Target:
- 2nd LHC shutdown (LS2): 2018-2019

Motivation:
- high precision measurements of rare probes at low $p_T$

Requirements:
- Large sample of events recorded on tape (accumulate $> 10 \text{ nb}^{-1}$ of Pb-Pb, plus pp and p-A data)
- Improved vertexing and tracking capabilities

Strategy:
- Upgrade of the Inner Tracking System (ITS)
- New Muon Forward Tracker (MFT)
- Upgrade of the Time Projection Chamber (TPC)
- Upgrade of Online systems, offline reconstruction and analysis framework
- Upgrade of the readout electronics of several detectors
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**ALICE ITS UPGRADE: OBJECTIVES**

- **Improve impact parameter resolution by a factor \( \sim 3 \) (5) \( r\text{-phi} \) (\( z \))**
  - Get closer to interaction point: 39 mm \( \rightarrow \) 22 mm (1\text{st} layer)
  - Reduce material budget: 1.14 \( X_0 \) % \( \rightarrow \) 0.3\% \( X_0 \) (inner layers)
  - Reduce pixel size: 50 \( \mu m \times 425 \mu m \) \( \rightarrow \) \( O(30 \mu m \times 30 \mu m) \)

- **High Standalone tracking efficiency and \( p_t \) resolution**
  - Increase granularity and radial extension: 6 \( \rightarrow \) 7 layers

- **Fast readout (now limited at 1kHz)**
  - Readout of Pb-Pb interactions at \( > 50 \) kHz
  - pp interactions at few hundred kHz

- **Fast insertion/removal for yearly maintenance**
  - Possibility to replace non functioning modules during yearly shutdown
THE NEW ITS LAYOUT

- Very thin sensors
- Very high granularity
- Large area to cover
- Moderate radiation levels

2 Barrels:
- 1 Inner: 3 (inner) layers
- 1 Outer: 4 (2 middle + 2 outer) layers

Radial coverage:
- 22 mm to 400 mm

Radiation Level (for the innermost layer, with a safety factor of 10):
- TID: 700 krad
- NIEL: $1 \times 10^{13}$ 1 MeV $n_{eq}$

- ~ 10 m² of silicon
- ~ 12.5 Gigapixels

Sensor choice
Monolithic silicon pixel sensors

Outer layers
Middle Layers
Inner Layers

Very thin sensors
Very high granularity
Large area to cover
Moderate radiation levels

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The ALICE experiment at CERN

Upgrade of the Inner Tracking System (ITS)

Pixel chip development: ALPIDE status & results
**Pixel Technology: Working Principle**

- 0.18μm CMOS imaging sensor process (from TowerJazz)

  - High resistivity epi-layer on p-type substrate
  - Special deep p-well layer to shield PMOS (true CMOS circuitry in the pixel)
  - (Possibility to use stitching)

**Optimization of NWELL diode output signal (V ~ Q/C):**

- Maximize Q
  - Limit the charge spread over adjacent pixels

- Minimize C
  - Small diode surface
  - Depleted volume

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### The ALPIDE Pixel Chip Development

**Pixel chip general requirements**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon Thickness</td>
<td>$\approx 50 , \mu m$</td>
</tr>
<tr>
<td>Intrinsic Spatial Resolution</td>
<td>$\approx 5 , \mu m$</td>
</tr>
<tr>
<td>Power density</td>
<td>$&lt; 100 , \text{mW/cm}^2$</td>
</tr>
<tr>
<td>Integration time</td>
<td>$&lt; 30 , \mu s$</td>
</tr>
<tr>
<td>Detection Efficiency</td>
<td>$&gt; 99%$</td>
</tr>
<tr>
<td>Fake Hit Rate</td>
<td>$&lt; 10^{-5}$</td>
</tr>
<tr>
<td>Chip size</td>
<td>$15 , \text{mm} \times 30 , \text{mm}$</td>
</tr>
<tr>
<td>Readout Type</td>
<td>digital</td>
</tr>
</tbody>
</table>

**Pixel chip development:**

- **ASTRAL (MISTRAL):** based on the experience of the STAR pxl detector (IPHC)
- **ALPIDE:** carried on by a collaboration formed by CCNU (Wuhan, China), CERN, INFN (Italy) and Yonsei (South Korea)

**Analog**
- Explorer-0
- Explorer-1

**Digital**
- pALPIDE
- pALPIDEfs
**PIXEL TECHNOLOGY: STARTING MATERIALS**

Wafers available on a variety of different starting materials (epi-layer of different thicknesses and resistivity)

<table>
<thead>
<tr>
<th>Type</th>
<th>Number of wafers</th>
<th>Epitaxial Thickness (µm)</th>
<th>Resistivity (kΩ cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 (LR-12)</td>
<td>3</td>
<td>12.0 ± 0.5</td>
<td>0.03</td>
</tr>
<tr>
<td>2 (HR-18)</td>
<td>4</td>
<td>18.0 ± 1.5</td>
<td>&gt;1</td>
</tr>
<tr>
<td>3 (HR-30)</td>
<td>3</td>
<td>30.0 ± 0.3</td>
<td>≈ 1</td>
</tr>
<tr>
<td>4 (HR-40A)</td>
<td>3</td>
<td>40.0 ± 0.6</td>
<td>≈ 1</td>
</tr>
<tr>
<td>5 (HR-20)</td>
<td>6</td>
<td>20.0 ± 1.9</td>
<td>6.2</td>
</tr>
<tr>
<td>6 (HR-40B)</td>
<td>3</td>
<td>40.0 ± 1.9</td>
<td>7.2</td>
</tr>
</tbody>
</table>

High Resistivity wafer types adopted for the ALPIDE R&D
EXPLORER FAMILY: DESCRIPTION

- **EXPLORER-0** and **EXPLORER-1**: first analog prototype chips of the ALPIDE family developed to
  - optimize charge collection and diode layout,
  - study the effect of back-biasing
  - study the sensitivity to radiation damage

- 2 sub-matrices
  - $90 \times 90$ array of $20 \ \mu m \times 20 \ \mu m$ pixels
  - $60 \times 60$ array of $30 \ \mu m \times 30 \ \mu m$ pixels

- 9 different electrode geometries (diode size, diode shape, spacing...)

- Expl-1: same circuit as Expl-0 but different input transistor geometry and routing
EXPLORER FAMILY: STARTING MATERIALS

- Test beam at DESY with 3-6 GeV $e^-$ and $e^+$ beams
- Cluster charge increases linearly with epi layer thickness
- Cluster size increases for thicker epi layer thickness
- Largest SNR (seed): HR-30 for $V_{bb} = -6V$, HR-20 for $V_{bb} = -1V$

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ALICE CERN-LHCC 2014-024
Test beam at DESY with 3-6 GeV $e^-$ and $e^+$ beams on irradiated samples

Chip irradiated at $10^{12}$, $3 \cdot 10^{12}$ and $10^{13}$ 1 MeV $n_{eq}$

Signal loss (at $10^{13}$ 1 MeV $n_{eq}$): $\approx 20\%$
PALPIDE

- **PALPIDE** is a small scale prototype chip used for the optimization of in-pixel front-end circuitry with a binary readout, and to address the feasibility of the priority encoding scheme

  - 64 × 512 pixels, 22 μm × 22 μm
  - In-pixel front-end
  - Binary readout
  - In-matrix sparsification

- Tested at DESY with 3-6 GeV e⁻ and e⁺ beams (SNR>20):
  - Detection efficiency: > 99%
  - Fake hit rate: ≈ 10⁻⁸/(event × pixel)
  - Spatial resolution: ≈ 5 μm

Perfect agreement with general requirements
pALPIDEfs: DESCRIPTION

- pALPIDEfs: large scale (30×15.3 mm²) prototype currently being characterized

- Explore microelectronics, architecture and system aspects
- 4 pixel types implemented (512×256)×4 pixels: 3 types with PMOS reset, 1 with diode reset

- Threshold: ~200 electrons
- Dispersion (RMS of threshold distribution) within one pixel type: ~ 16-19 electrons
PALPIDEFs: HIT MAP

Preliminary results
CONCLUSIONS

- The new ALICE ITS will be installed during LS2 in 2018-2019

- It will consist of 7 layers of Monolithic Pixel Sensors

- An intense R&D effort is being carried out:
  - Different diode layouts, epi-layer thicknesses and resistivity have been compared
  - Adequate detection efficiency, spatial resolution and radiation hardness have been shown

  We are on the right track!

- A full scale digital prototype is currently under study
Material budget distribution across the Inner Barrel Stave (bottom) and a detail of the overlapping staves (top)
<table>
<thead>
<tr>
<th></th>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>9.13</td>
<td>284</td>
<td>-</td>
<td>2.5</td>
<td>29.4</td>
<td>108</td>
</tr>
<tr>
<td>1</td>
<td>6.13</td>
<td>174</td>
<td>-</td>
<td>1.53</td>
<td>24.5</td>
<td>144</td>
</tr>
<tr>
<td>2</td>
<td>4.47</td>
<td>121</td>
<td>-</td>
<td>1.06</td>
<td>21.3</td>
<td>180</td>
</tr>
<tr>
<td>3</td>
<td>0.31</td>
<td>14</td>
<td>196</td>
<td>0.76</td>
<td>33.6</td>
<td>88</td>
</tr>
<tr>
<td>4</td>
<td>0.20</td>
<td>12</td>
<td>168</td>
<td>0.65</td>
<td>36.7</td>
<td>112</td>
</tr>
<tr>
<td>5</td>
<td>0.10</td>
<td>11</td>
<td>144</td>
<td>0.98</td>
<td>78.8</td>
<td>160</td>
</tr>
<tr>
<td>6</td>
<td>0.08</td>
<td>10</td>
<td>139</td>
<td>0.95</td>
<td>87.2</td>
<td>184</td>
</tr>
</tbody>
</table>
EFFICIENCY AND FAKE HIT RATE

![Graph showing efficiency and fake hit rate vs. a cut parameter. The graph includes data points and error bars for different conditions, such as -1V 20×20 and -6V 20×20, with corresponding efficiency and fake hit rate values.]
- Pixel capacitance drops with increasing reverse bias

- Effect similar for all starting materials → Minor influence of epi layer